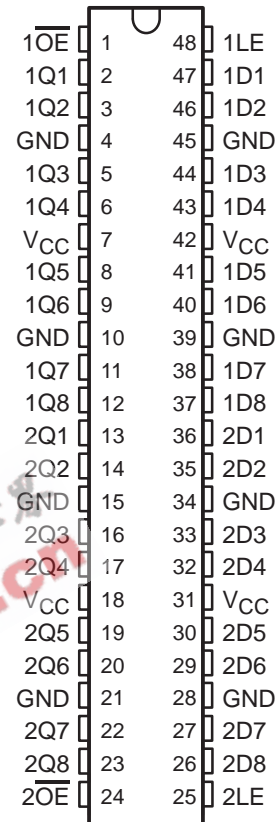


54AC16373, 74AC16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus*™ Family
- 3-State True Outputs
- Full Parallel Access for Loading
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

54AC16373 . . . WD PACKAGE
74AC16373 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16373 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16373 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC16373 is characterized for operation from -40°C to 85°C .



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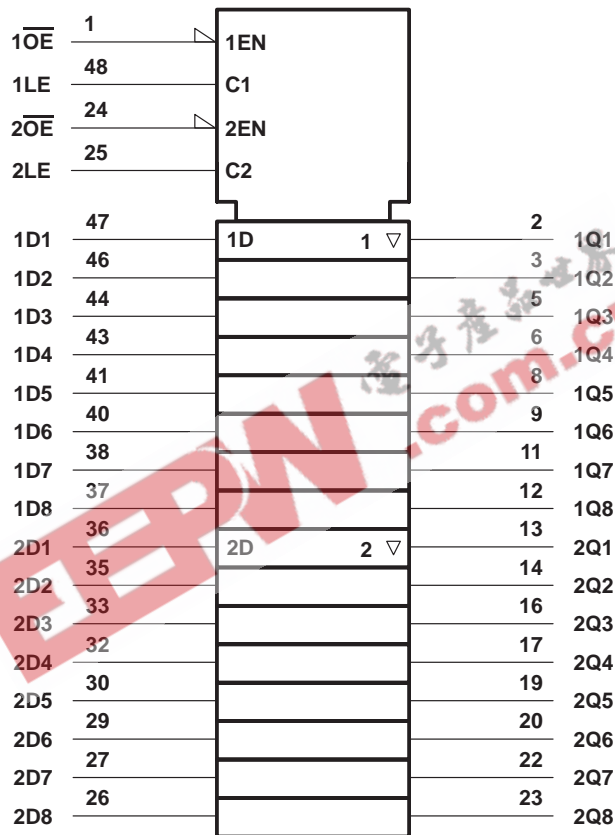
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SCAS121B – MARCH 1990 – REVISED APRIL 1996

FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†

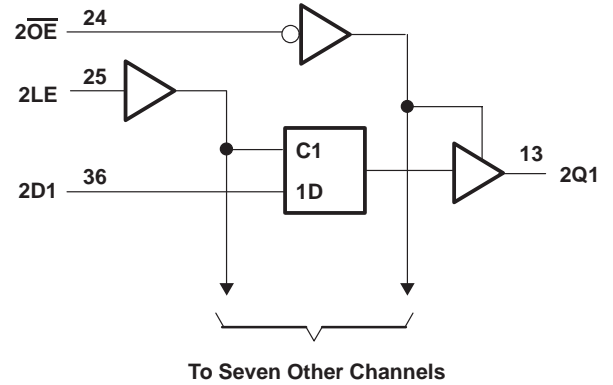
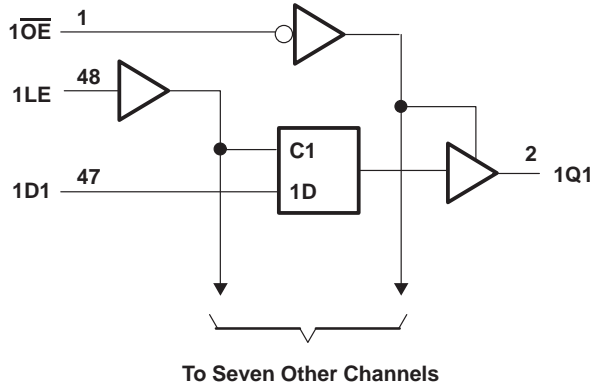


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

54AC16373, 74AC16373
16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCAS121B – MARCH 1990 – REVISED APRIL 1996

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

54AC16373, 74AC16373

16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCAS121B – MARCH 1990 – REVISED APRIL 1996

recommended operating conditions (see Note 3)

		54AC16373			74AC16373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V		2.1	2.1		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 5.5 V		3.85	3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9		V	
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
V _I	Input voltage	0		V _{CC}	0	V _{CC}	V	
V _O	Output voltage	0		V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 3 V			-4		mA	
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12		mA	
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
Δt/Δv	Input transition rise or fall rate	0		10	0	10	ns/V	
T _A	Operating free-air temperature	-55		125	-40	85	°C	

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
I _{OH} = -75 mA [†]	5.5 V				3.85		3.85			
V _{OL}	I _{OL} = 50 μA	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	I _{OL} = 12 mA	3 V				0.36		0.44		
		4.5 V				0.36		0.44		
		5.5 V				0.36		0.44		
I _{OL} = 24 mA	5.5 V					1.65	1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5	±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	80	μA	
C _i	V _I = V _{CC} or GND	5 V			4.5				pF	
C _o	V _O = V _{CC} or GND	5 V			12				pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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SCAS121B – MARCH 1990 – REVISED APRIL 1996

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

		T _A = 25°C		54AC16373		74AC16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	5		5		5		ns
t _{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t _h	Hold time, data after LE↓	3		3		3		ns

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T _A = 25°C		54AC16373		74AC16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	4		4		4		ns
t _{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t _h	Hold time, data after LE↓	2.5		2.5		2.5		ns

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	3.7	10.6	13.4	3.7	15.1	3.7	15.1	ns
t _{PHL}			4.3	11.3	14	4.3	14.8	4.3	14.8	
t _{PLH}	LE	Q	4.6	12.9	15.8	4.6	18.6	4.6	18.6	ns
t _{PHL}			4.5	12.1	14.6	4.5	16.4	4.5	16.4	
t _{PZH}	\overline{OE}	Q	4.2	11.8	14.8	4.2	17.5	4.2	17.5	ns
t _{PZL}			5.4	16.3	19.8	5.4	22.3	5.4	22.3	
t _{PHZ}	\overline{OE}	Q	4.2	7.9	9.5	4.2	10.2	4.2	10.2	ns
t _{PLZ}			3.8	7.1	8.9	3.8	9.8	3.8	9.8	

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	3.1	6.7	8.5	3.1	9.7	3.1	9.7	ns
t _{PHL}			3.5	7.3	9.1	3.5	10.1	3.5	10.1	
t _{PLH}	LE	Q	3.8	8.2	10.2	3.8	11.9	3.8	11.9	ns
t _{PHL}			3.6	7.8	9.7	3.6	10.9	3.6	10.9	
t _{PZH}	\overline{OE}	Q	3.5	7.4	9.4	3.5	10.8	3.5	10.8	ns
t _{PZL}			4.3	9.1	11.3	4.3	12.8	4.3	12.8	
t _{PHZ}	\overline{OE}	Q	3.9	6.6	8	3.9	8.8	3.9	8.8	ns
t _{PLZ}			3.7	5.9	7.4	3.7	8.1	3.7	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	C _L = 50 pF, f = 1 MHz	43	pF
	Outputs disabled	5			

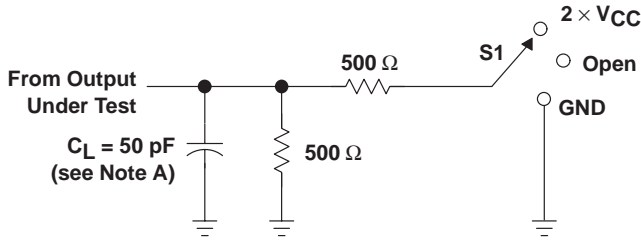
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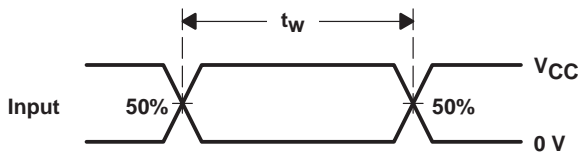
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PARAMETER MEASUREMENT INFORMATION

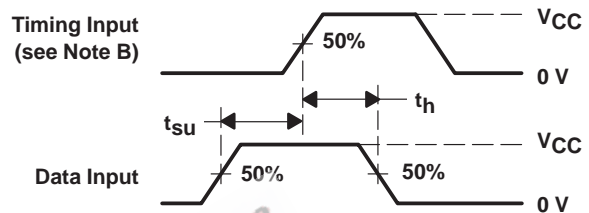


LOAD CIRCUIT

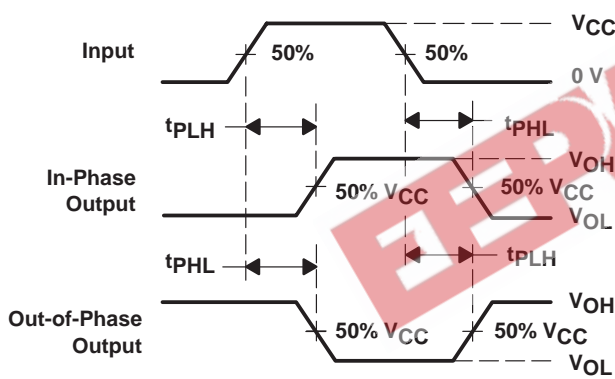
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



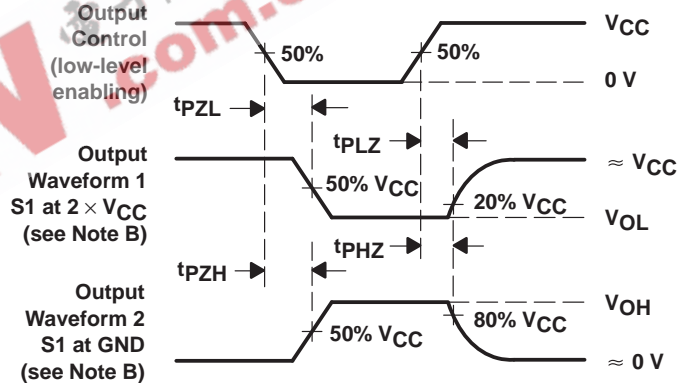
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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