

# FAN8025G3

## 5-Channel Motor Driver

### Features

- 2-Channel BTL drivers with current feedback
- 2-Channel BTL DC motor drivers
- 1-Channel Logic input loading driver
- Built-in thermal shutdown circuit
- Built-in mute circuit
- Operating supply voltage: 4.5~13.2V

### Description

The FAN8025G3 is a monolithic IC, suitable for 2-ch BTL DC motor drivers, 2-ch motor drivers with current feedback which drive the focus and the tracking actuator and 1-ch logic input loading driver.



### Typical Applications

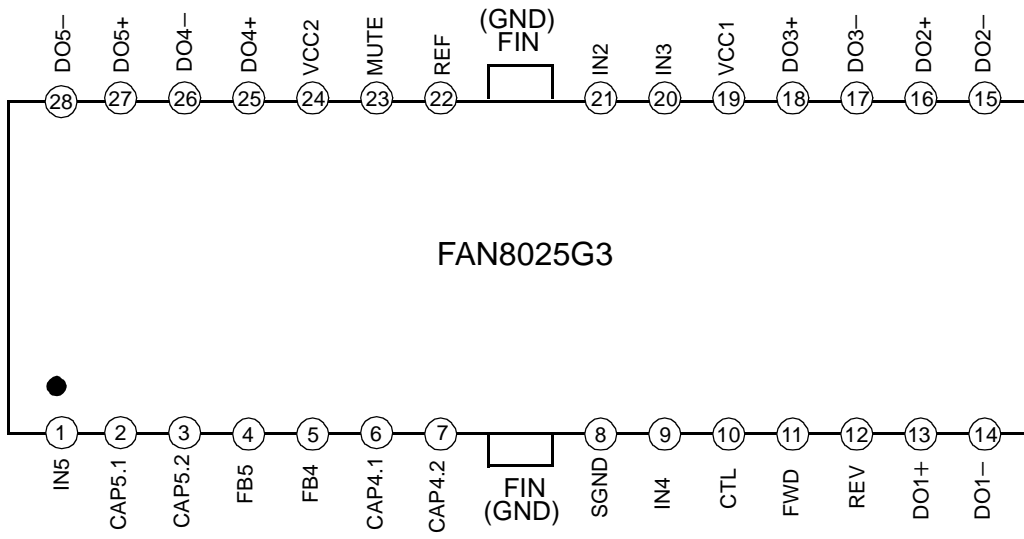
- Compact disk ROM (CD-ROM)
- Digital video disk player (DVDP)
- Video compact disk player (VCDP)
- Other compact disk media

### Ordering Information

Device	Package	Operating Temp.
FAN8025G3	28-SSOPH-375SG2	-35 °C ~ 85 °C
FAN8025G3X	28-SSOPH-375SG2	-35 °C ~ 85 °C

X:Tape & Reel type

## Pin Assignments

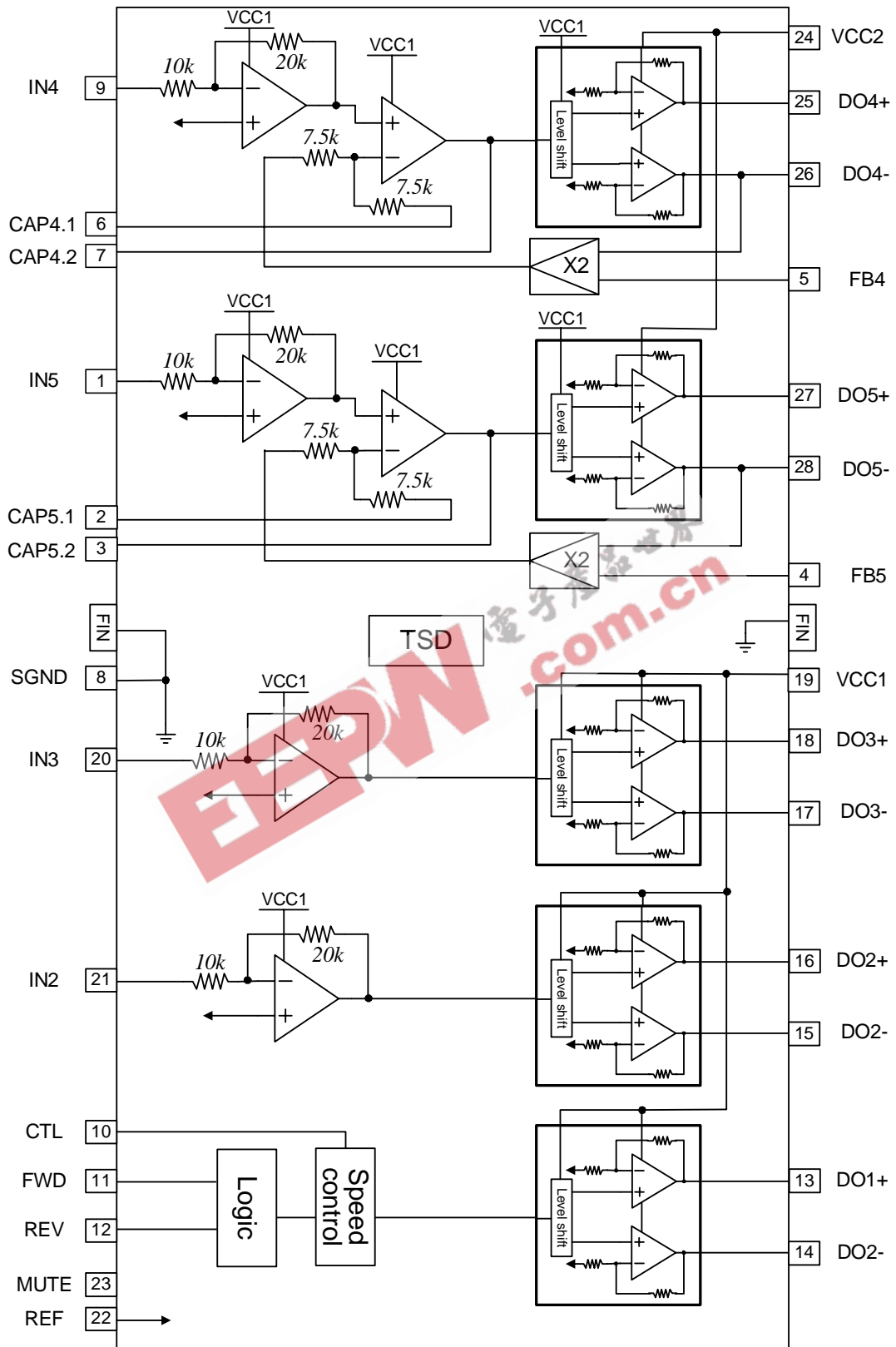


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## Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	IN5	A	CH5 input
2	CAP5.1	A	Connection with capacitor for CH5
3	CAP5.2	A	
4	FB5	A	Feedback for CH5
5	FB4	A	Feedback for CH4
6	CAP4.1	A	Connection with capacitor for CH4
7	CAP4.2	A	
8	SGND	P	Signal ground
9	IN4	A	CH4 input
10	CTL	A	CH1 speed control input
11	FWD	I	CH1 forward input
12	REV	I	CH1 reverse input
13	DO1+	O	Drive1 Output (+)
14	DO1-	O	Drive1 Output (-)
15	DO2-	O	Drive2 Output (-)
16	DO2+	O	Drive2 Output (+)
17	DO3-	O	Drive3 Output (-)
18	DO3+	O	Drive3 Output (+)
19	VCC1	P	Power for channel 1,2 and 3
20	IN3	A	CH3 input
21	IN2	A	CH2 input
22	REF	A	Bias voltage input
23	MUTE	I	CH2,3,4 and 5 mute signal input
24	VCC2	P	Power for channel 4 and 5
25	DO4+	O	Drive4 Output (+)
26	DO4-	O	Drive4 Output (-)
27	DO5+	O	Drive5 Output (+)
28	DO5-	O	Drive5 Output (-)

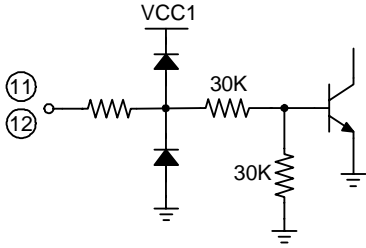
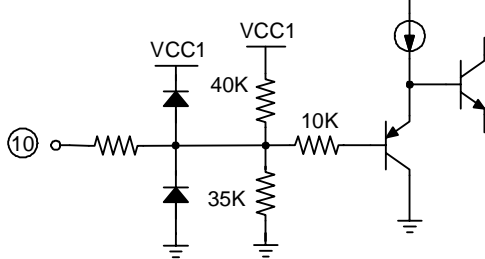
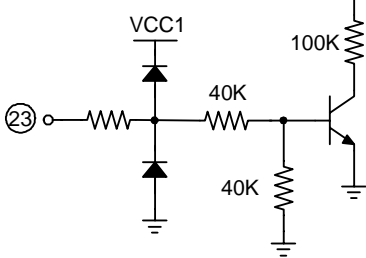
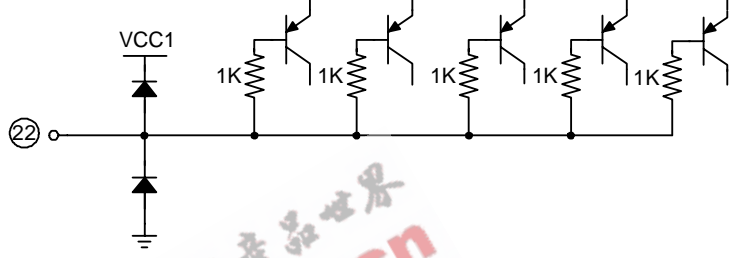
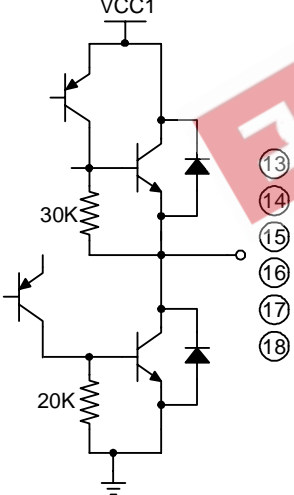
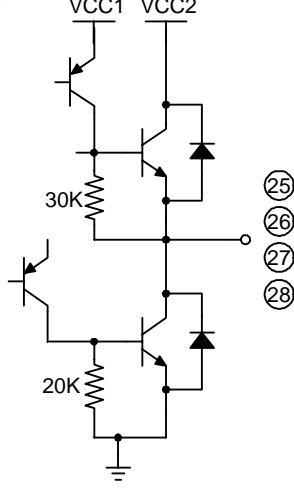
# Internal Block Diagram



## Equivalent Circuits

CH2/3/4/5 Inputs	Current Feedback Amp Outputs
Current Feedback Amp Compensation Inputs	
Current Feedback Inputs	

### Equivalent Circuits(continued)

CH1 Inputs(FWD/REV)	CH1 Control Input(CTL)
	
Mute Input	Ref Input
	
CH1/2/3 Drive Outputs	CH4/5 Drive Outputs
	

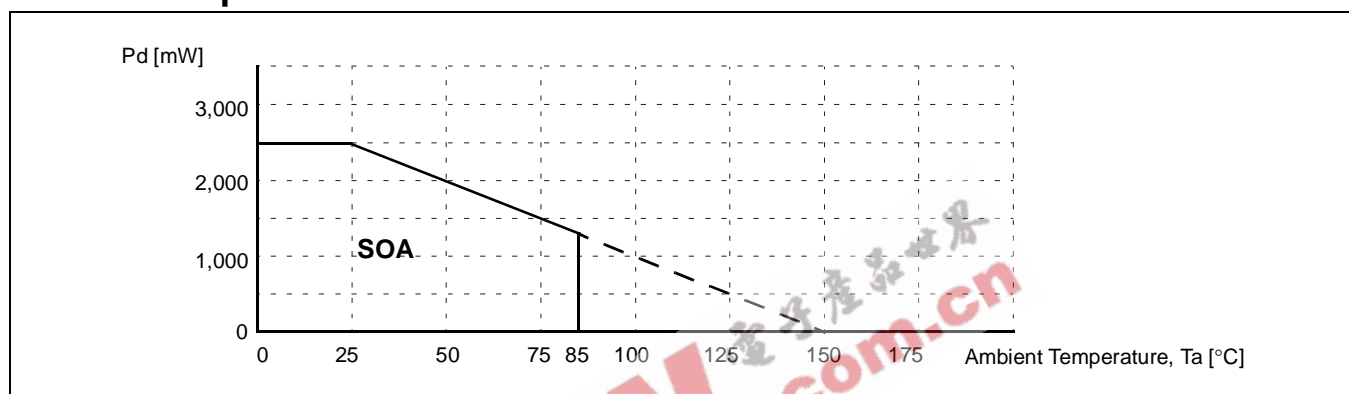
## Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	$V_{CC1,2max}$	15	V
Power dissipation	$P_D$	2.5 <sup>note</sup>	W
Operating temperature range	$T_{OPR}$	-35 ~ +85	°C
Storage temperature range	$T_{STG}$	-55 ~ +150	°C

### NOTE:

1. When mounted on a 50mm × 50mm × 1mm PCB (Phenolic resin material).
2. This is experimental data.
3. Power dissipation decrease rate : -20mW/°C(Ta≥25°C).
4. Should not exceed  $P_D$  and SOA (Safe Operating Area).

## Power Dissipation Curve



## Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{CC1,2}$	4.5	-	13.2	V

## Electrical Characteristics

(Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{CC1} = 12\text{V}$ ,  $V_{CC2} = 5\text{V}$  & the other conditions & nomenclatures follow the test circuit)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent Current1	ICC1	Stand-by off	-	18	27	mA
Quiescent Current1	ICC2	Stand-by on	-	9	-	mA
Mute On Voltage	V <sub>MON</sub>	-	-	-	0.5	V
Mute Off Voltage	V <sub>MOFF</sub>	-	2.0	-	-	V
REF input voltage range	V <sub>REFIN</sub>	-	1.0	-	3.3	V
REF input current range*	I <sub>REFIN</sub>	V <sub>REF</sub> =1.65V	-10	-	10	uA
<b>ACTUATOR DRIVER(CH4,CH5)</b>						
Output Offset Current45	I <sub>OO45</sub>	-	-6	0	+6	mA
Maximum Output Voltage45	V <sub>OM45</sub>	-	3.6	4.0	-	V
Transconductance	G <sub>M45</sub>	V <sub>IN</sub> = 100mVp-p, f=1kHz	1.2	1.4	1.6	A/V
Control voltage input range45*	V <sub>IN45</sub>	-	0	-	5	V
<b>SLED/SPINDLE DRIVER(CH2,CH3)</b>						
Output Offset Voltage23	V <sub>OF23</sub>	-	-100	0	+100	mV
Maximum Output Voltage23	V <sub>OM23</sub>	-	9.5	10.0	-	V
Closed loop Voltage Gain23	G <sub>VLO23</sub>	V <sub>IN</sub> = 100mVp-p, f=1kHz	16	18.0	20	dB
Control voltage input range23*	V <sub>IN23</sub>	-	0	-	5	V
<b>LOADING DRIVER(CH1)</b>						
Input high level Voltage	V <sub>IH</sub>	-	2	-	-	V
Input low level Voltage	V <sub>IL</sub>	-	-	-	0.5	V
Output Offset Voltage1	V <sub>OF1</sub>	-	-50	0	50	mV
Transfer Gain	G <sub>V</sub>	-	1.0	1.2	1.4	V/V

\* : Guaranteed design values



## Application Information

### 1. Reference Input

- Reference input (PIN 22)

The applied voltage at the reference input pin must be ranged between 1.0V and 3.3V, when  $V_{CC1}=12V$ .  
When the reference input voltage goes below 0.7V, all channels are disabled.

### 2. Stand-by Function

- MUTE input (PIN 23)

We recommend CH1 as the loading(or tray) motor driver. Detailed logic table is as below.

INPUT LOGIC		CH1	CH2	CH3	CH4	CH5
Stand-by input	High	O	O	O	O	O
	Low or open	O	X	X	X	X

### 3. Protection Function

Thermal shutdown (TSD)

When the chip temperature rises above 175°C, the thermal shutdown (TSD) circuit is activated and the output circuit is in the mute state, that is off state. The TSD circuit has a temperature hysteresis of 25°C

### 4. Separation Of Power Supply

- VCC2 (PIN 24)

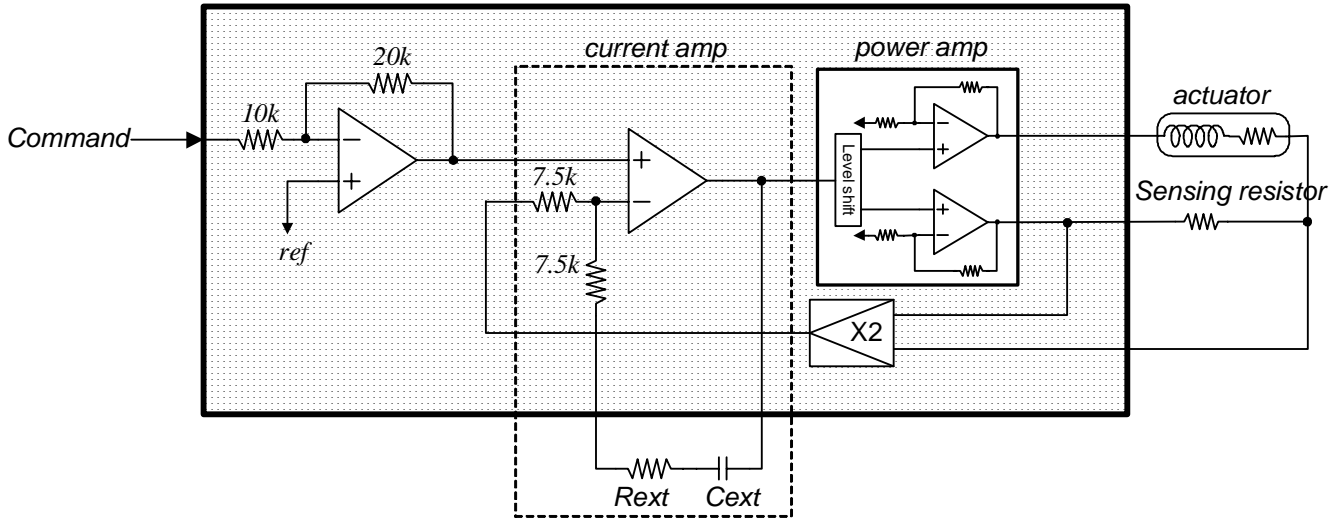
VCC2 is the power supply for CH4 and CH5, which are current feedback drivers.

- VCC1 (PIN 19)

VCC1 is the power supply for CH1, CH2, CH3 and predriver.

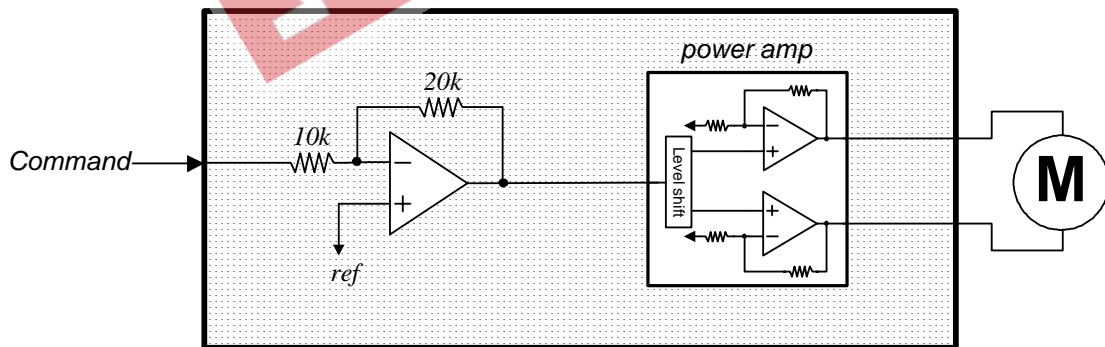
**VCC1 input voltage must be higher than or same to VCC2. ( $V_{CC1} \geq V_{CC2}$ )**

4. Current feedback channels(channel 4 & 5)



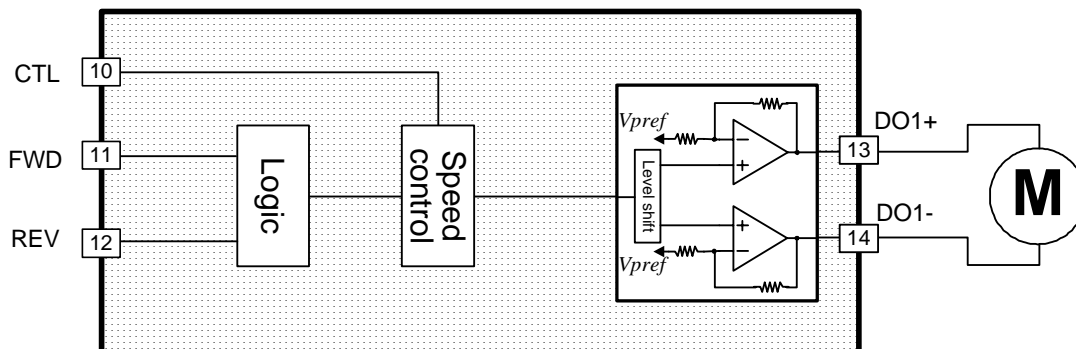
- The reference voltage(ref) is given externally through pin 22.
- The input OP-amp output signal is amplified by (20K/10K) times and then fed to the current feedback amplifier.
- The current feedback amplifier compares the output current sensed input and command input then makes the controlled output to eliminate delay effect of the load. Please refer to the application note for more information about current feedback theory(<http://www.fairchildsemi.com/an/AN/AN-4109.pdf>).
- The DC gain of current feedback amplifier and power amplifier is unity, that is 1 [A/V]. Users can change the gain by adding external resistor at the command input.

5. Channel 2 & 3 schematic



- The reference voltage(ref) is given externally through pin 22.
- The input OP-amp output signal is amplified by (12K/10K) times and then fed to the power amplifier. The gain of power amplifier is 4 so the total max gain of channel 2 and 3 is 8.

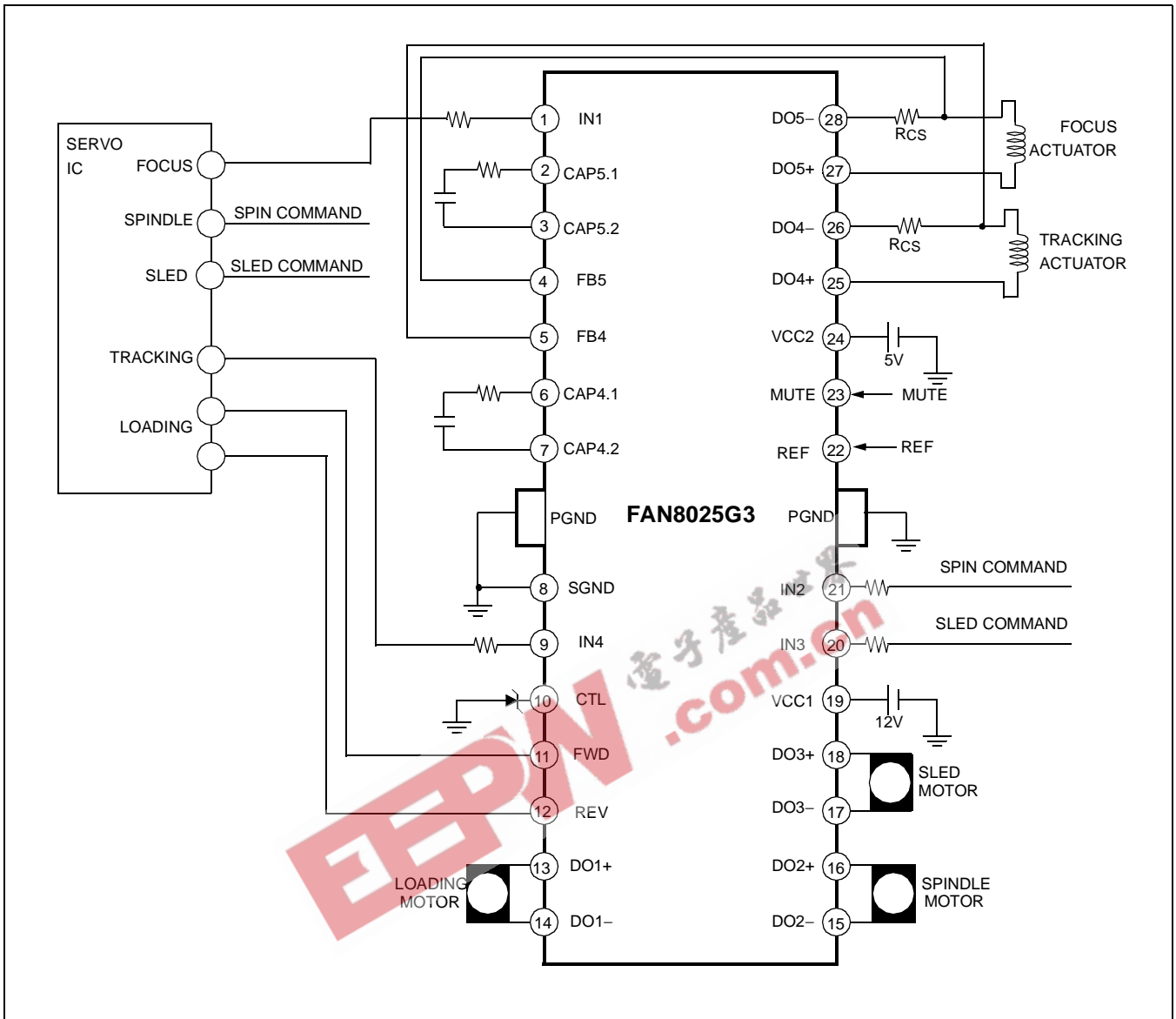
6. Channel 1 schematic



- The inputs of channel 1 are FWD, REV which are logic inputs and CTL which is linear input. The CTL input is used to control the output gain, meanwhile FWD and REV are logic inputs to select output driver's direction.
- Below table is FWD and REV logic input table.

Input		Output		
FWD	REV	DO1+	DO1-	condition
H	H	$V_{pref}$	$V_{pref}$	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	$V_{pref}$	$V_{pref}$	Brake

## Typical Application Circuits





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