DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT112

Dual JK flip-flop with set and reset; negative-edge trigger

Product specification
Supersedes data of December 1990
File under Integrated Circuits, IC06

1998 Jun 10

Philips Semiconductors

PHILIPS

Dual JK flip-flop with set and reset; negative-edge trigger

74HC/HCT112

FEATURES

- Asynchronous set and reset
- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT112 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT112 are dual negative-edge triggered JK-type flip-flops featuring individual nJ, nK, clock ($n\overline{CP}$), set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) inputs.

The set and reset inputs, when LOW, set or reset the outputs as shown in the function table regardless of the levels at the other inputs.

A HIGH level at the clock ($n\overline{CP}$) input enables the nJ and nK inputs and data will be accepted. The nJ and nK inputs control the state changes of the flip-flops as shown in the function table. The nJ and nK inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.
Output state changes are initiated by the HIGH-to-LOW transition of $n\overline{CP}$.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	$n\overline{CP}$ to nQ, $n\overline{Q}$		17	19	ns
	$n\overline{S}_D$ to nQ, $n\overline{Q}$		15	15	ns
	$n\overline{R}_D$ to nQ, $n\overline{Q}$		18	19	ns
f_{max}	maximum clock frequency		66	70	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

Dual JK flip-flop with set and reset; negative-edge trigger

74HC/HCT112

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC112D; 74HCT112D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC112DB; 74HCT112DB	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC112N; 74HCT112N	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC112PW; 74HCT112PW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	set inputs (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 7	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
15, 14	$1\overline{R}_D$, $2\overline{R}_D$	reset inputs (active LOW)
16	V_{CC}	positive supply voltage

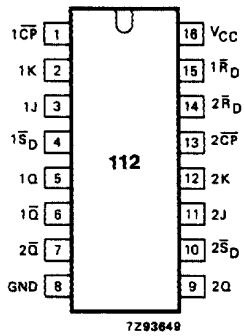


Fig.1 Pin configuration.

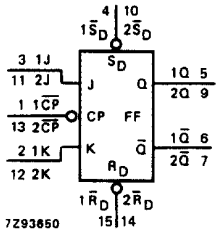


Fig.2 Logic symbol.

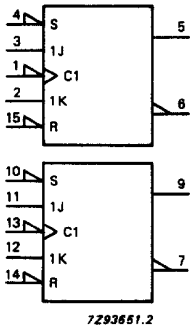


Fig.3 IEC logic symbol.

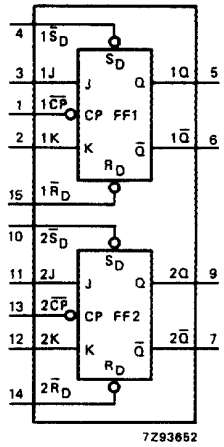


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	L
toggle	H	H	↓	h	h	$\overline{q}$	q
load “0” (reset)	H	H	↓	l	h	L	H
load “1” (set)	H	H	↓	h	l	H	L
hold “no change”	H	H	↓	l	l	q	$\overline{q}$

Note

1. If $n\overline{S}_D$ and $n\overline{R}_D$ simultaneously go from LOW to HIGH, the output states will be unpredictable.
   H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
   X = don’t care
   ↓ = HIGH-to-LOW CP transition

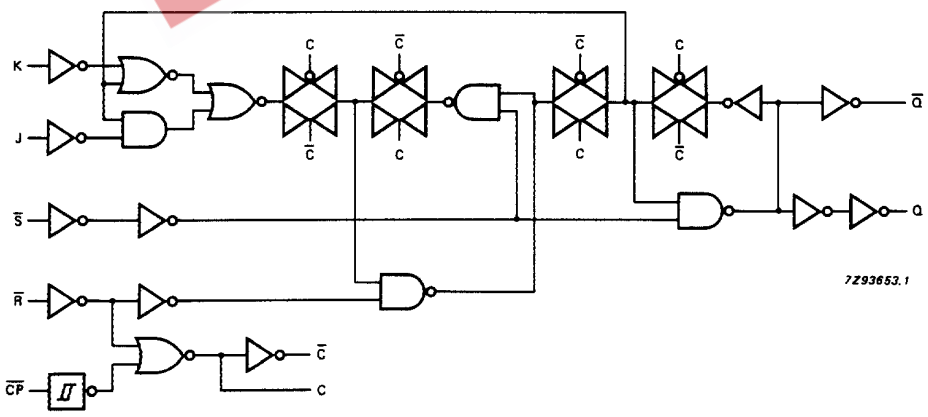


Fig.5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		50 18 14	155 31 26		295 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	set or reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	80 16 14	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	80 16 14	−19 −7 −6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.6
f_{max}	maximum clock pulse frequency	6 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

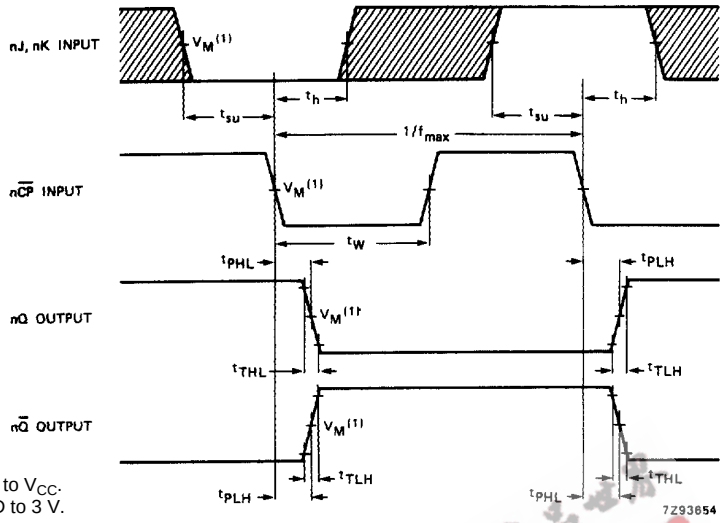
INPUT	UNIT LOAD COEFFICIENT
$1\overline{S}_D$, $2\overline{S}_D$	0.5
1K, 2K	0.6
$1\overline{R}_D$, $2\overline{R}_D$	0.65
1J, 2J	1
$1\overline{CP}$, $2\overline{CP}$	1

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		21	35		44		53	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		23	40		50		60	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		22	37		46		56	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		18	32		40		48	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig.6
t_W	set or reset pulse width LOW	18	10		23		27		ns	4.5	Fig.7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	20	11		25		30		ns	4.5	Fig.7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	20	−8		25		30		ns	4.5	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	16	7		20		24		ns	4.5	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	0	−7		0		0		ns	4.5	Fig.6
f_{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig.6

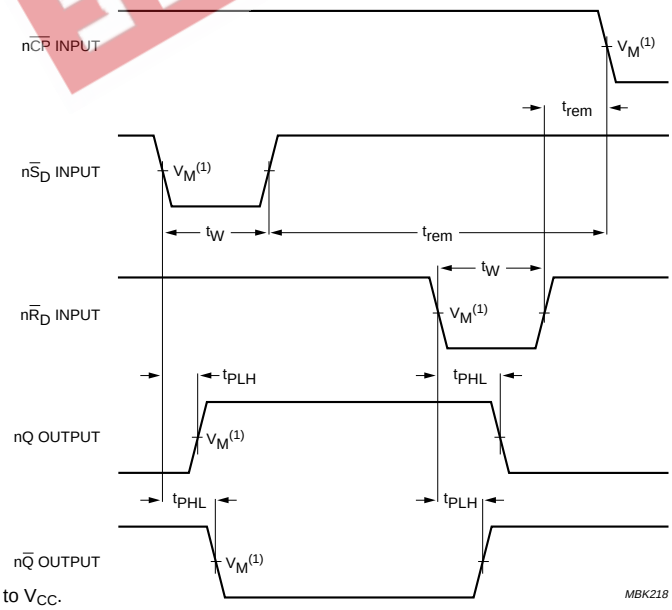
AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nJ, nK to $n\overline{CP}$ set-up times, the $n\overline{CP}$ to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.

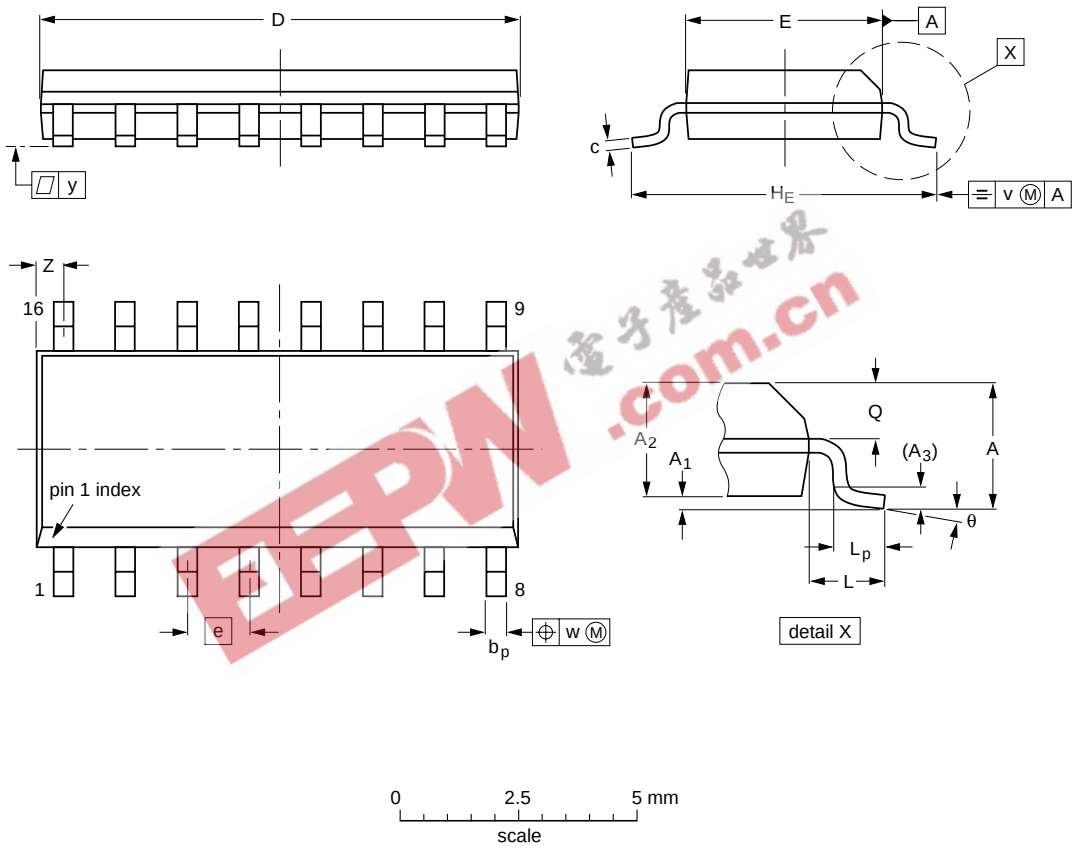


(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse width and the $n\overline{R}_D$ and $n\overline{S}_D$ to $n\overline{CP}$ removal time.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

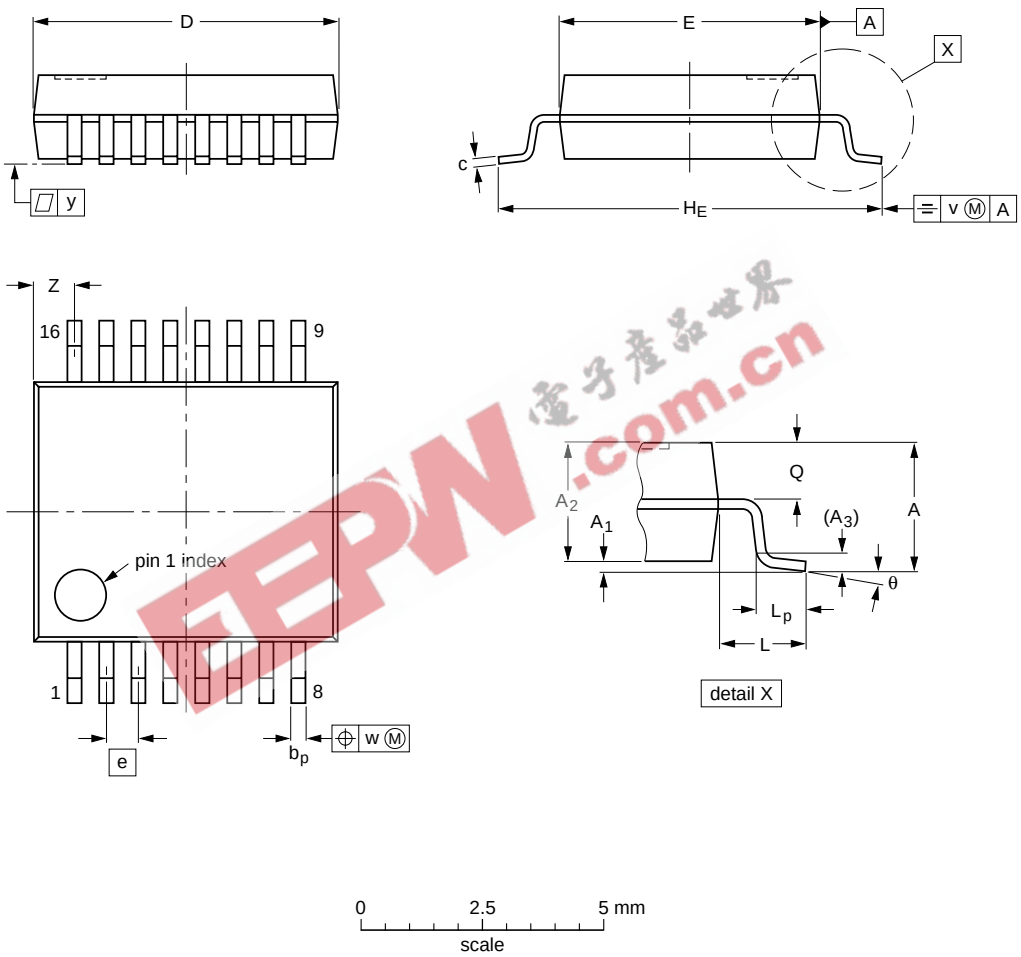
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

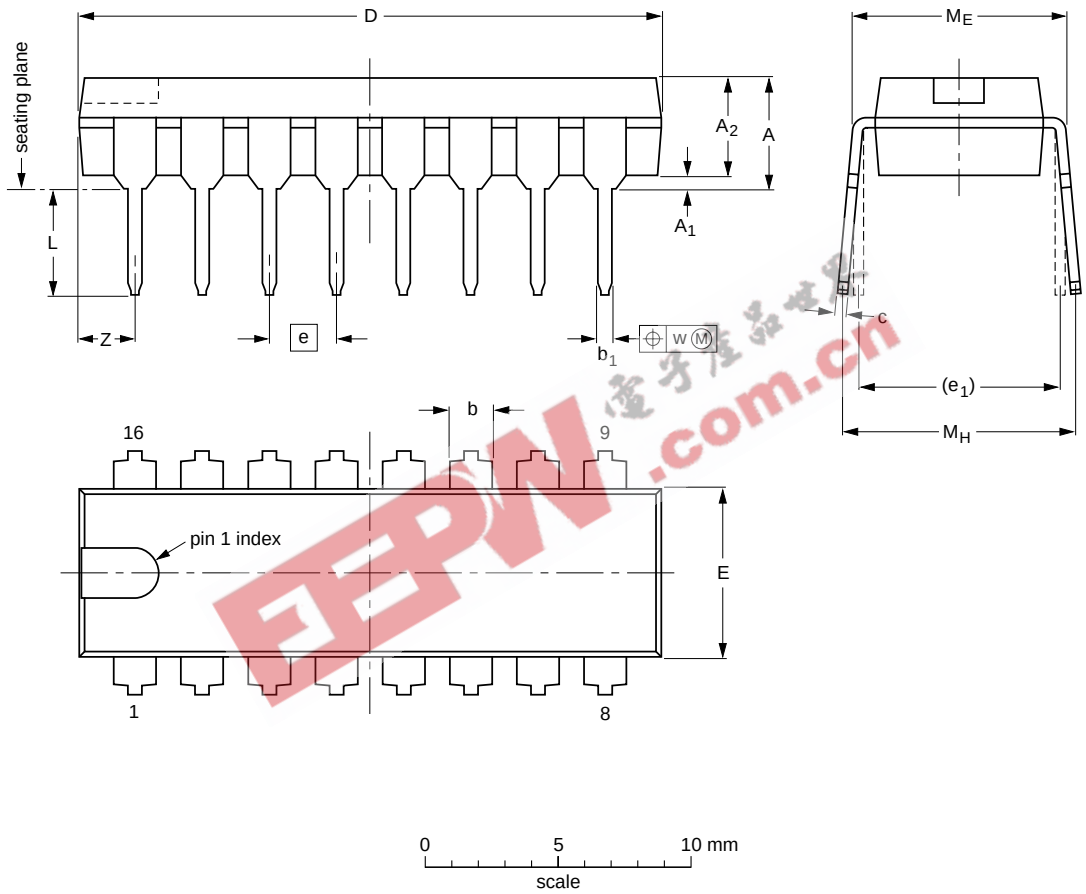
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

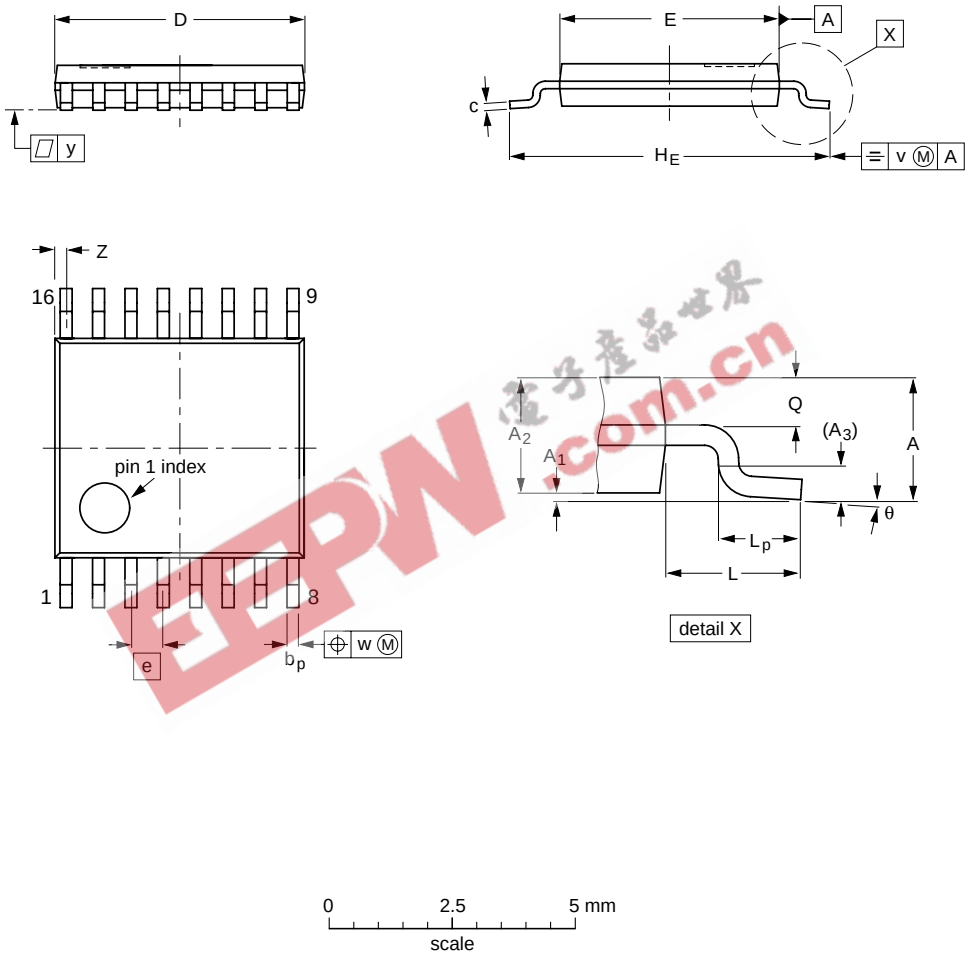
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO, SSOP and TSSOP

Reflow soldering

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

Even with these conditions:

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in

one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.